LOW COST UTSI® TECHNOLOGY FOR RF WIRELESS APPLICATIONS

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ABSTRACT

Ultra Thin Silicon (UTSi) IC technology has been developed for RF, analog, and digital signal applications. The technology is based on low cost CMOS VLSI technology with fully integrated passive components. The insulating substrate provides high isolation and high quality passive components, paving the way for on-chip matching elements. For the first time, excellent high-speed/high-frequency performance is simultaneously demonstrated by the highly integrated UTSi technology.

INTRODUCTION

The desire to achieve high level of integration, the need to decrease power consumption, the migration toward smaller dimensions, and the consumer-driven market are spurring the interest in low cost Si-based technology. However, there are two basic limitations that can not be addressed through lithography improvements in standard CMOS process. The nonlinear parasitic capacitances between the MOSFET and substrate, as well as the low resistivity substrate, can not be eliminated from the bulk CMOS process. The nonlinear capacitances will degrade the linearity required for wireless systems. The low resistivity substrate results in strong coupling through the substrate and poor quality passive components. The UTSi technology has been developed to overcome this limitation.

UTSi technology is a CMOS process with roots in decades of government sponsored research. Recently, UTSi CMOS has been perfected, and can be manufactured in an unmodified CMOS fabrication facility [1]. Fig. 1 sketches cross sections of MOSFETs implemented in a submicron bulk CMOS and UTSi CMOS processes. The basic transistor structures are the same except that wells, well contacts, isolated regions and substrate contacts are not required in the UTSi device. Unlike, other Silicon-On-Insulator (SOI) technologies, UTSi has a completely insulating substrate. The insulating substrate provides the required isolation to accommodate RF circuits, analog-to-digital converters and digital logic circuitry in addition to the good quality passive components [2].

In this paper, the UTSi technology will be briefly reviewed. The active device characteristics will be presented. The high frequency performance will be summarized. The potential application for RF-mixed mode will be also described.

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UTSI TECHNOLOGY

UTSi technology is based on a low power, low cost CMOS VLSI technology with the addition of fully integrated high quality passive components. An improved thin-film silicon, with 1000 A^o thickness, is epitaxially grown on sapphire substrate. Solid-phase epitaxy (SPE) regrows the defect-free silicon downward from the surface, removing the defects and resulting in high effective mobility. The process consists of LOCOS field oxidation, 0.5 dual doped polycide gate with 100 Å gate oxide, and three layers of metal. The transistors are fully depleted with multiple threshold voltages in the range of 0 to +/- 1 V.

Standard CMOS processing is used. The number of process steps are less than bulk CMOS. The process is qualified to commercial standards in plastic packages. UTSi CMOS takes advantage of decades of advances in CMOS manufacturing cost effectiveness. The technology is capable of providing the system-on-chip solution.

TRANSISTOR PERFORMANCE

The DC characteristics of intrinsic (IN) UTSi CMOS is shown in Fig. 2 and Fig. 3. The low carrier life time in UTSi technology, about 1 nsec, and fully depleted transistor result in superior performance compare to other SOI technologies. Moreover, the very low diffusivity of dopants in the crystalline alumina substrate prevents dopant loss to the underlying dielectric, eliminating one of the major cause of threshold voltage variation. Table I summarize the UTSi transistors types and their dc characteristics. The fully depleted operation improves the low-voltage performance, especially when compared to bipolar or standard CMOS transistors.

The gain and h_{21} are plotted in Fig. 4 for IN 0.5 μm multifinger UTSi CMOS (W/L= 250 μm/0.5 μm) at V_{ds} and I_{ds} equals to 2.5 V and 15 mA, respectively. The transistor has the following properties: finger width less than 20 μm, oxide thickness t_{ox} of 100 A^o and polycide sheet resistance of 8 ohm/square. The f_T and f_{max} of the UTSi MOSFET equal to 17 GHz and 50 GHz, respectively. The high f_{max} value for UTSi CMOS compared to standard bulk CMOS is due to the elimination of the nonlinear parasitic drain and source to bulk capacitors and the fully depleted nature of UTSi transistors. Fig. 5 presents the noise figure and maximum gain of IN and NL UTSi MOSFET transistors (W/L= 250 μm/0.5 μm) at 5 mA drain current versus frequency. The maximum gain for both transistors is the same and equal to 12 dB at 2 GHz. The IN and NL MOSFET transistors have noise figure F_{min} of 0.55 and 0.6 dB at 2 Ghz. The aforementioned data is consistent with the RF transistor performance required for wireless applications.

One of the most striking features of UTSi CMOS transistors is their extremely high linearity for RF mixing operation. This can be explained by the small variation in the input capacitance with input voltage compared to other FET technologies, the superior square law characteristics of the UTSi transistor in addition to the reasons previously mentioned for high f_{max}. Fig. 6 presents the conductances gm and gds associated with 0.8x500 μm IN and NL UTSi transistors versus drain current. These data are extracted from s-parameters measurement at 1 Ghz. In UTSi MOSFET, the bulk charge is minimal and fully eliminated in the accumulation and depletion regions of the transistor. Circuit performance implemented on UTSi technology are reported elsewhere [4]-[5].

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RF MIXED MODE APPLICATIONS

Wireless communication system-on-a-chip requires integration of digital, analog and RF mixed-signal CMOS. Fig. 7 shows unloaded ring oscillator propagation delay versus drain voltage for UTSi and bulk CMOS technologies. The 0.65 and 0.35 μm effective length UTSi offers lower delay than the 0.5 and 0.25 μm bulk, respectively. Moreover, the 0.35 μm effective length (L_{eff}) UTSi CMOS technology presents high-speed performance over the entire voltage range from below 1V to above 3V. It is clear that the fully-depleted transistor operation and dielectric isolation give approximately 1.5 generations of speed advantage over bulk CMOS.

A key advantage of UTSi technology is the inherent isolation provided by the insulating substrate and the high quality of on-chip passive component [2]. Moreover, this technology takes advantage of decades of advances in VLSI CMOS manufacturing. Therefore, high yield UTSi paves the way for integrating digital, analog, and RF functions on a single-silicon-chip with competitive price due to area savings and reduced processing steps compared to bulk CMOS in addition to lower testing and packaging cost due to high level of integration.

CONCLUSION

UTSi CMOS IC technology has been developed to provide the cost and performance requirements of future integrated one-chip solution for wireless communication systems. The transistor RF performance meets the requirement for high frequency systems. The insulating substrate and the high quality on-chip passive component are ideal for wireless applications. Results show that the technology has potential applications for low power system-on-a-chip solutions.

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TABLE I . UTSi MOSFET transistor types and DC characteristics.

Type	IN	NL	RN	IP	PL	RP
V_{th} (mV)	50	300	800	-50	-300	-800
g_m(μS/μm)	30.8	29.8	26.2	12.9	11.0	9.02
I_{dsat}(μA/μm)	683	477	330	347	288	136
L_{eff}(μm)	0.35	0.35	0.35	0.35	0.35	0.35

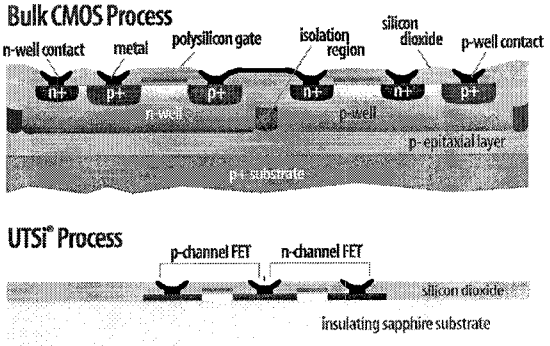

Fig. 1 Sketches of MOSFETs implemented in a typical submicron bulk CMOS and UTSi CMOS processes.

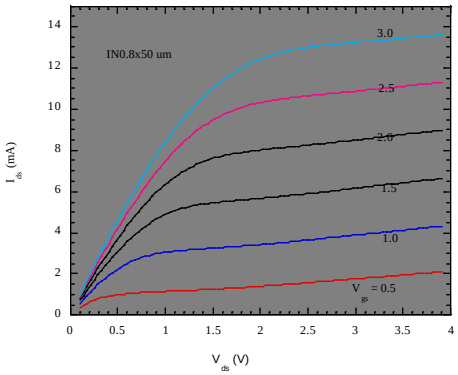

Fig. 2 Output dc characteristics of intrinsic IN 0.8x50 mm UTSi MOSFET.

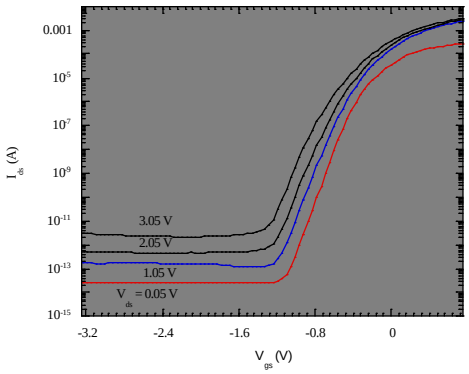

Fig. 3 Output subthreshold characteristics of intrinsic IN 0.8x50 mm UTSi MOSFET.

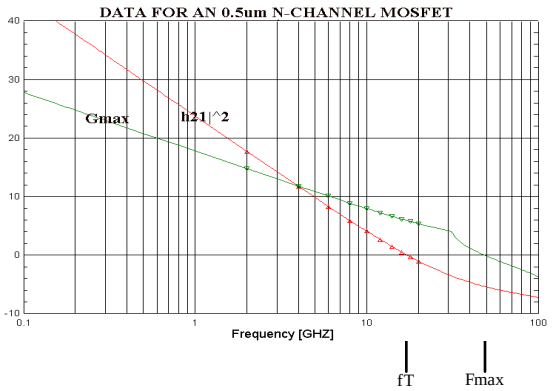

Fig. 4 Gain and h_{21} IN 0.5 μm multifinger UTSi CMOS (W/L= 250 μm/0.5 μm) at 15 mA drain current.

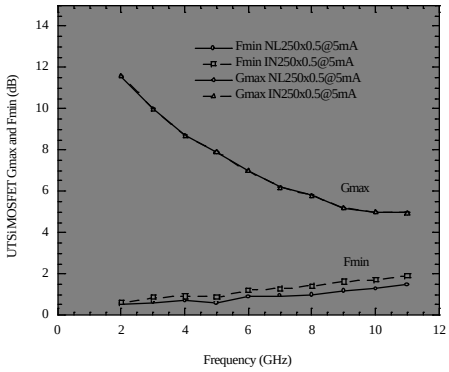

Fig. 5 Noise figure and Gmax of IN and NL transistors (W/L= 250 μm/0.5 μm) at 5 mA drain current.

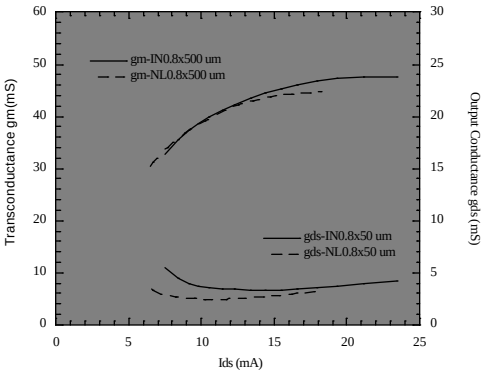

Fig. 3 Conductances for 0.8x500 μm IN and NL UTSi transistors at 1 GHz.

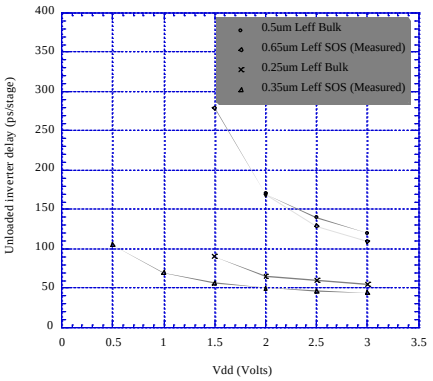

Fig. 7 Unloaded ring oscillator propagation of UTSi and bulk CMOS technologies.